REMARKS

Claims 1, 2 and 5-16 were pending in the application. Claims 3, 4 and 17-23 have been canceled in previous amendments. Claims 1, 2, 5-13 and 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yao et al. and Satou et al. Claims 2 and 5-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yao and Satou as applied to claim 1, and further in view of Radogna et al. Claims 14 and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yao and Satou as applied to claims 1 and 15, and further in view of Muller et al. Claims 1 and 15 have been amended, and claim 2 has been canceled, leaving claims 1 and 5-16 presently under consideration. Reconsideration and reexamination of the application in view of the amendments and following remarks is respectfully requested.

The present invention is directed to enabling data communication between a storage area network and another network implementing a different protocol. Two microsequencer systems are employed to perform translations between the two different protocols. For example, one microsequencer system may be employed to perform a translation from a first to a second protocol, and the other microsequencer system may perform a translation from the second to the first protocol. Each microsequencer system may include one or more microsequencers cooperatively connected together to perform the translation using Very Long Instruction Words (VLIW) from an instruction memory for processing multiple instructions in parallel. Each VLIW contains a plurality of instruction fields executable in parallel by different instruction units within the microsequencer. The instruction memory is loadable via a processor interface to make the *microsequencers programmable to accommodate different first and second network protocols.*

Claims 1, 2, 5-13 and 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yao and Satou. Claim 2 has been canceled, rendering the rejection of claim 2 moot. With regard to claims 1, 5-13 and 15, this rejection is respectfully traversed.

In Applicants' previous response, claims 1 and 15 were amended to recite the limitation of first and second microsequencer systems/processing elements including one or more microsequencers/functional units. The present Office Action now cites Yao for the first time, and

states that this limitation is obvious in view of Yao and Satou because "Yao et al. teaches a plurality of translation systems including one or more translation devices."

Yao discloses a number of *translation or routing tables* needed for address translation between network devices utilizing different protocols. For example, Yao discloses a translation table 205 in FIG. 9 which is used by addressing software when transmitting a frame from a Fibre Channel host to an iSCSI device (paragraph [0050]), and when transmitting a frame from an iSCSI host to a Fibre Channel device (paragraph [0052]). Other *translation or routing tables* for performing different translations are shown in FIGs. 11, 12, 13, 17 and 18 of Yao.

However, the different tables disclosed in Yao are merely unrelated collections of associated addresses operated upon by addressing software. In other words, Yao takes a brute force approach of simply using a different translation table to perform different protocol translations. In contrast, the microsequencers/functional units as recited in claims 1 and 15 are far more complex and interrelated because they *cooperate* in the translation process and are together capable of executing fields in a Very Long Instruction Word (VLIW) *in parallel* to execute a plurality of instructions in a single instruction cycle. Tables and microsequencers/functional units are thus very different entities that cannot be equated or analogized, and it would not have been obvious at all from the simple unrelated translation tables disclosed Yao to implement the feature of multiple microsequencers/functional units operating cooperatively and in parallel as recited in claims 1 and 15. To conclude otherwise amounts to an impermissible attempt to reconstruct the claimed invention in hindsight using nonanalogous art.

Because neither Yao nor Satou, alone or in combination, discloses, teaches or suggests all of the limitations of claims 1 and 15, it is respectfully submitted that the rejection of claims 1 and 15 under 35 U.S.C. §103(a) as being unpatentable over Yao and Satou has been traversed. In addition, because claims 5-13 depend from claim 1, the rejection of those claims is traversed for the same reasons provided above with respect to claim 1.

Notwithstanding the above, claims 1 and 15 have been amended to further distinguish Yao and Satou. Claims 1 and 15 have been amended to recite "the instruction memory being loadable via a processor interface to make the [microsequencers/functional units] *programmable* to accommodate different first and second network protocols." Support for these amendments can be found on page 2, lines 17-18, page 8 lines 13-17, and page 18 lines 14-17 of the specification.

As noted above, Yao discloses the use of different translation tables, each one uniquely created to perform a particular protocol translation. Because each of the translation tables performs a particular function, the translation tables in Yao are not programmable. Neither Yao nor Satou contains any disclosure at all related to multiple programmable microsequencers/functional units as recited in claims 1 and 15.

Therefore, for this additional reason, neither Yao nor Satou, alone or in combination, discloses, teaches or suggests all of the limitations of amended claims 1 and 15, and it is respectfully submitted that the rejection of amended claims 1 and 15 under 35 U.S.C. §103(a) as being unpatentable over Yao and Satou has been overcome. In addition, because claims 5-13 depend from claim 1, the rejection of those claims has been overcome for the same reasons provided above with respect to claim 1.

Claims 2 and 5-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yao and Satou as applied to claim 1, and further in view of Radogna. Claim 2 has been canceled, rendering the rejection of claim 2 moot.

Claims 5-13 depend from claim 1. As explained above, neither Yao nor Satou, alone or in combination, discloses, teaches or suggests all of the limitations of claim 1. Furthermore, Radogna fails to make up for the deficiencies of Yao or Satou.

Radogna fails to disclose, teach or suggest cooperating programmable microsequencers each having access to an instruction memory, as recited in amended claim 1. Radogna discloses only a *single* microsequencer 100 (see FIG. 3 of Radogna) for performing header translation for frames being moved from an input FIFO to an output FIFO. Because Radogna is a unidirectional

system, it understandably fails to disclose, teach or suggest a second microsequencer for header translation of frames being moved in the opposite direction. Furthermore, it would *not* have been obvious to one skilled in the art to simply provide another microsequencer for performing header translation for frames being moved in the opposite direction, because the invention as recited in claim 1 does not simply recite two microsequencers. Rather, claim 1 recites two microsequencer systems with a *cooperative* relationship between microsequencers in the microsequencer systems, and that the microsequencers have *access to a common instruction memory*.

Therefore, even if one skilled in the art would have been motivated to combine Yao, Satou and Radogna, none of those references discloses, teaches or suggests first and second microsequencer systems for performing protocol conversion in both directions, or that the microsequencers in those systems act cooperatively with each other and access a common instruction memory, as recited in claim 1.

Because neither Yao, Satou nor Radogna, alone or in combination, discloses, teaches or suggests all of the limitations of claim 1, and because claims 5-13 depend from claim 1, it is respectfully submitted that the rejection of claims 5-13 under 35 U.S.C. §103(a) as being unpatentable over Yao, Satou and Radogna has been overcome.

Claims 14 and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yao and Satou as applied to claims 1 and 15, and further in view of Muller. Claim 14 depends from amended claim 1, and claim 16 depends from amended claim 15.

As described above, neither Yao nor Satou, alone or in combination, discloses, teaches or suggests first and second microsequencer systems/processing elements for performing protocol conversion in both directions, or that the microsequencers/functional units in those systems cooperatively with each other and access a common instruction memory, and that the instruction memory is loadable via a processor interface to make the microsequencers/processing elements *programmable* to accommodate different first and second network protocols, as recited in amended claims 1 and 15.

Furthermore, Muller fails to make up for the deficiencies of Yao and Satou. Muller is directed to a network interface for receiving a packet from a network and transferring it to a host computer system. The header of a packet may be parsed by a *single* microsequencer located in a parser module 106 (see FIG. 1A and col. 24 lines 12-67). Muller does not translate between two different network protocols in both directions, and therefore fails to disclose, teach or suggest a second microsequencer for parsing headers in packets in a different protocol.

Therefore, even if one skilled in the art would have been motivated to combine Yao, Satou and Muller, none of those references discloses, teaches or suggests first and second processing elements for performing protocol conversion in both directions, or that the functional units in those processing elements cooperatively with each other and access a common instruction memory, as recited in claims 1 and 15.

Because neither Yao, Satou nor Muller, alone or in combination, discloses, teaches or suggests all of the limitations of claims 1 and 15, and because claim 14 depends from claim 1 and claim 16 depends from claim 15, it is respectfully submitted that the rejection of claims 14 and 16 under 35 U.S.C. §103(a) as being unpatentable over Yao, Satou and Muller has been overcome.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If, for any reason, the Examiner finds the application other than in condition for allowance, Applicants request that the Examiner contact the undersigned attorney at the Los Angeles telephone number (213) 892-5752 to discuss any steps necessary to place the application in condition for allowance.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, Applicants petition for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing Docket No. 491442004500.

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Respectfully submitted,

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